

REMARKS

Application acknowledges receipt of the Office Action dated May 31, 2007. Claims 1-30 are pending. Claims 8, 10-30 were rejected under 35 U.S.C. §112 second paragraph. Claims 1-30 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent Publication No. 2004/0044833 to Ryan ("Ryan") and U.S. Patent No. 5,502,621 to Schumacher et al. ("Schumacher"). Claims 1-30 were provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over copending U.S. Patent Application No. 11/417,389 to Janzen ("Janzen") in view of Ryan and Schumacher. Claims 1-20 and 22-30 were further rejected obvious over claim 37 of Janzen in view of Ryan and Schumacher.

Rejections Under 35 U.S.C. §112

Claims 8 and 10-30 stands rejected as being indefinite for reciting the phrases "substantially parallel" and "substantially abutting." Applicant respectfully asserts that the cited phrase is not indefinite. The word "substantially" has been interpreted by the Federal Circuit as meaning "largely but not wholly that which is specified." *Playtex Products, Inc. v. Procter & Gamble Co.*, 400 F.3d 901, 906 (Fed. Cir. 2005). The Federal Circuit has further held that "substantial" is not indefinite. *Liquid Dynamics*, 355 F.3d 1361, 1368 (Fed. Cir. 2004) ("The term 'substantial' is a meaningful modifier implying 'approximate' rather than 'perfect.'"); *Anchor Wall Systems, Inc. v. Rockwood Retaining Walls, Inc.*, 340 F.3d 1298, 1311 (Fed. Cir. 2003) ("[T]erms such as 'approach each other,' 'close to,' 'substantially equal,' and 'closely approximate' are ubiquitously used in patent claims and that such usages, when serving reasonably to describe the claimed subject matter to those of skill in the field of the invention and to distinguish the claimed subject matter from the prior art, have been accepted in patent examination and upheld by the courts").

The specification need not specify what is meant by words of approximation. In particular, the Federal Circuit has interpreted the phrase "generally parallel" to be sufficiently definite without any further definition:

The written description does not specify any special definition for the terms 'generally,' 'parallel,' or the phrase 'generally parallel.' See, e.g., 015 patent, col. 5, ll. 5-6 ('The top surface 26 generally lies parallel to the bottom surface 28.');

713 patent, col. 5, ll. 10-11 (same). Moreover, nothing in the prosecution

history of the 015 patent family clearly limits the scope of “generally parallel” such that the adverb “generally” does not broaden the meaning of parallel. Accordingly, we hold that the phrase ‘generally parallel’ envisions some amount of deviation from exactly parallel.

Anchor Wall Systems, Inc. v. Rockwood Retaining Walls, Inc., 340 F.3d 1298, 1311 (Fed. Cir. 2003).

However, notwithstanding the definiteness of the word “substantially,” in order to expedite prosecution, claims 10, 14, 21, 26, 27, and 29 have been amended to remove the word “substantially.”

Double Patenting Rejection

Claims 1-30 stand provisionally rejected under the judicially created doctrine of obviousness-type double patenting in view. Applicant respectfully asserts that an obviousness-type double patenting rejection is improper. As discussed below, the combination of Schumacher and Ryan is not suggested in the prior art and therefore the claims are not obvious in view of the claims of Ryan.

Discussion of the Disclosed Embodiment

The disclosed embodiments of the invention will now be discussed in comparison to the prior art. Of course, the discussion of the disclosed embodiments, and the discussion of the differences between the disclosed embodiments and the prior art subject matter, do not define the scope or interpretation of any of the claims. Instead, such discussed differences merely help the Examiner appreciate important claim distinctions discussed thereafter.

The present application is directed toward solving the problem of skew in signals transmitted between memory chips and a memory hub. Skew results when differences in path length cause signals to arrive at different times rather than simultaneously. *Specification*, at page 1, lines 19-26 (*Specification* attached hereto as Exhibit B). Skew may cause errors due to lack of synchronization. *Id.*

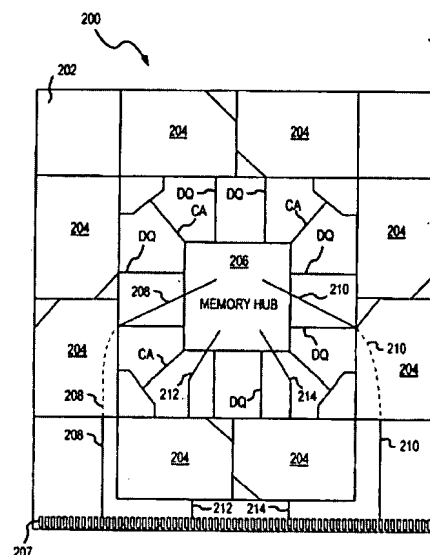


FIG.2

Embodiments of the invention include pairs of memory devices surrounding a memory hub. Each memory device is coupled to the memory hub by a control-address bus and a data bus. The memory devices are arranged in pairs with one of the memory devices of the pair rotated 180 degrees relative to the other memory device of the pair such that their first ends are adjacent one another. *Specification*, page 7, lines 24-26. As shown in Figure 2 (reproduced to the right) the memory devices (204) have first and second ends with data pins (DQ) located near one end and control-address pins (CA) near the other end. *Specification*, page 7, lines 14-18. Inasmuch as the ends having the data pins are adjacent one another, data busses extending to each memory device of the pair may therefore be parallel to one another and have the same length. *Specification*, page 7, lines 26-29. By maintaining an equal path length, the amount of skew is reduced.

The control-address busses extend at an angle relative to the data bus toward the second ends of the memory devices. *Specification*, page 8, lines 5-8. As is apparent in Figure 2, the address bus of each memory device is parallel to the address bus of an adjacent memory device of the adjacent pair of memory devices and is the same length. Thus, each address bus of each memory device is the same length and control-address signals will arrive substantially simultaneously at each memory device, thereby reducing errors due to skew.

The disclosed embodiments therefore provide a means for accommodating different distances between a memory hub and the different ends of a memory device while still maintaining substantially equal path lengths for signals of the same type for all the memory devices coupled to the memory hub.

Discussion of the Cited References

Schumacher discloses a system in which integrated circuits (IC) are designed such that the pin assignments are substantially mirrored about an axis. The ICs are mounted to a circuit board such that one IC is rotated 180 degrees relative to another IC mounted some distance therefrom. Likewise, an IC may mount on an opposite side of the circuit board and rotate 180 degrees from another IC. Schumacher teaches only integrated circuits arranged in rows, rather than surrounding a memory hub. Schumacher fails to teach that integrated circuits on the same side of the circuit board abut one another or are arranged in pairs that are perpendicular to adjacent pairs.

Schumacher teaches that this arrangement enables leads to be “routed in the same direction and less likely to have cross over problems.” Col. 2, lns. 57-59. The teachings of Schumacher do not suggest modification of Ryan. As shown in Ryan (Figure 2 of Ryan is reproduced to the left), individual buses radiate outwardly from the memory hub and directly connect each memory device to the memory hub without crossing. There is therefore no possibility of crossover and no simplification would occur from using the arrangement of Schumacher. One skilled in the art would not see any use for using the arrangement of Schumacher with the device of Ryan – it would require rearrangement and reengineering without achieving the improvement claimed by Schumacher. It therefore would not be obvious to combine Schumacher and Ryan to achieve the disclosed embodiment.

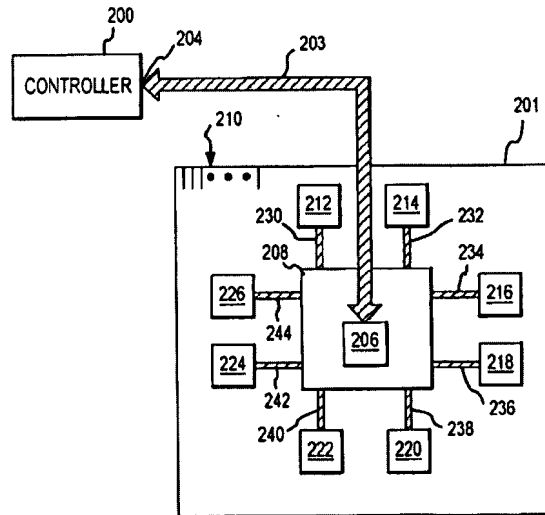


FIG.2

Furthermore, neither Schumacher nor Ryan teach arranging control-address lines at an angle relative to data lines. As is apparent from Figure 2 of Ryan, the buses extend directly from the memory hub to the devices. Ryan does not teach buses of differing angles extending to the same memory device. Ryan actually teaches against this approach. Ryan teaches that the arrangement disclosed is an alternative to devices which, for example, “increase path lengths of [a] command/address bus coupled to the [first] devices to make them equal to the command/address bus to the [second] devices.” ¶ 10 (reference numbers omitted). Ryan further teaches that coupling memory devices “directly to the memory hub over the shortest path possible between each memory device and the memory hub.” ¶ 25.

To modify the buses of Ryan such that the control-address lines were at an angle relative to the data lines would require reengineering without any suggestion of a benefit in the cited references. There is no indication in Ryan or Schumacher that placing data and control lines at different orientations would provide any benefit.

Discussion of the Claims

Turning now to the claims, the patentably distinct differences between the cited references and the claim language will be specifically pointed out.

With respect to claim 1, none of the cited references teach or suggest, in combination with the other limitations of claim 1, a memory module including “a plurality of memory devices positioned around the memory hub and arranged in pairs on the same side of the circuit board as one another, each memory device having the same physical pin layout and including pins associated with a first functional group of signals adjacent a first end of each memory device and pins associated with a second functional group of signals adjacent a second end of each memory device, and the first end of each memory device in each pair being positioned adjacent one another on the circuit board and the second end of each device in a pair being positioned adjacent a second end of a device in one of the other pairs.” (emphasis added).

With respect to claim 10, none of the cited references teach or suggest, in combination with the other limitations of the claim, a memory module having “a plurality of memory devices positioned around the memory hub and arranged in pairs on the same side of the circuit board as one another, each memory device having the same physical pin layout and including pins associated with a first functional group of signals adjacent a first end of each memory device and pins associated with a second functional group of signals adjacent a second end of each memory device, and the first ends of each memory device in each pair being positioned abutting one another on the circuit board.” (emphasis added).

With respect to claim 14, none of the cited references teach or suggest a memory module including “four pairs of devices, each pair being positioned perpendicular to adjacent pairs and located adjacent a respective edge of the circuit board, and wherein the first functional group of signals comprise data signals and the second functional group of signals comprise control-address signals.” (emphasis added).

With respect to claim 21, none of the cited references teach or suggest, in combination with the other limitations of the claim “a plurality of memory devices positioned around the memory hub and arranged in pairs on the same side of the circuit board as one another, each memory device having the same physical pin layout and including pins associated with a first functional group of signals adjacent a first end of each memory device and pins

associated with a second functional group of signals adjacent a second end of each memory device, and the first ends of each memory device in each pair abutting one another on the circuit board." (emphasis added).

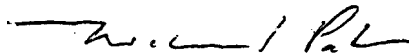
With respect to claim 26, none of the cited references teach or suggest, in combination with the other limitations of the claim, a method including the step of "positioning pairs of memory devices around the memory hub such that both devices in each pair are on the same side of the circuit board and each pair is perpendicular to adjacent pairs, each memory device in a respective pair being physically rotated 180 degrees in the plane of the circuit board relative to the other device in the pair." (emphasis added).

Claims 2-9, 11-13, 15-20, 22-25, and 27-30 are allowable as dependent on allowable claims 1, 10, 21, and 26, respectively.

All of the claims remaining in the application are clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,

DORSEY & WHITNEY LLP



Michael G. Pate
Registration No. 53,439
Telephone No. (206) 903-2398

MGP:sp

Enclosures:

Postcard
Fee Transmittal Sheet (+ copy)
Supplemental Information Disclosure Statement
Form PTO-1449

DORSEY & WHITNEY LLP
1420 Fifth Avenue, Suite 3400
Seattle, Washington 98101-4010
(206) 903-8800 (telephone)
(206) 903-8820 (fax)